REMARKS

Claims 1-6, 10-15, and 27-41 are all the claims pending in the application. Claims 16-22 were withdrawn and cancelled pursuant to a restriction requirement dated February 13, 2004. Claims 7-9 and 23-26 were withdrawn and cancelled pursuant to a restriction requirement dated June 30, 2004. This Amendment amends claims 3,27, 31-35, 39, and 40, and addresses each point of objection and rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

Applicants thank the Examiner for initialing the Information Disclosure Statements filed August 16, 2004 and November 22, 2004.

Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 1-6 and 10-15 are allowed, and for indicating that claims 28, 37, and 38 would be allowable if rewritten in independent form. Applicants request that the rewriting of claims 28, 37, and 38 be held in abeyance until the Examiner has had the opportunity to reconsider the allowability of parent claims 27 and 35.

Specification Amendments

The specification is amended to correct reference numbers that were inconsistent with the drawings. Support for each of these changes can be found by comparing the drawings to the text of the specification.

Claim Objections

In view of the Examiner's comments, Applicants have amended claims 27 and 31 in an effort to avoid logical ambiguity. Claim 27 now recites:

> terminating ~~the foregoing~~ performance of the outputting and the decoding operations of the instruction processing system, if any, that result from the providing of the address to the instruction processing system.

Claim 31 now recites:

> terminating performance of the outputting [[,]] and the converting operations of the second cache, if any, that result from the applying of the address to the second cache.

§ 112 Rejections

Claims 32, 33, and 34 are amended to provide antecedent basis.

To address ambiguity regarding cache units, claim 35 is amended to recite that the instruction caches has "a first cache lookup unit and a data fetch unit," while claim 39 is amended to recite that the UOP cache comprises "a second cache lookup unit and a cache fetch unit..."

§ 102 Rejections - Claims 31, 33, 35, 36, and 39

Claims 31, 33, 35-36, and 39 are rejected under 35 U.S.C. § 102(b) as being anticipated by Friendly *et al.,* "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism" ("Friendly").

The Examiner asserts that "the gate effectively terminates operations of the circuit above it."

Applicants respectfully submit that the Examiner's assertion is technically inaccurate. The three-state buffer between the Instruction Cache Decoder and the Core serves as a simple switch, having the effect of either opening or closing a path from the output of the Decoder to the Core. Although their output may not reach the Core if the Trace Cache has a hit, the operations of the Instruction Cache and the Decoder are otherwise unabated.

At least because Friendly does not disclose the "terminating" step in independent claim 31, nor a "hit/miss indicator to selectively *disable* the data fetch unit" as recited in independent claim 35, claims 31, 33, 35, 36, and 39 are not anticipated. Withdrawal of the § 102(b) rejection is requested.

§ 102 Rejections - Claims 27 and 31

Claims 27 and 31 are rejected under 35 U.S.C. § 102(a) as being anticipated by "the admitted prior art."

The Examiner asserts that terminating the operations of the instruction processing system (claim 27) and the second cache (claim 31) is "inherent since the express purpose of utilizing the UOP cache is to avoid if possible the latency involved with accessing un-decoded instructions via the instruction cache."

The Examiner's assertion of inherency appears to be based upon the same line of reasoning put forward for Friendly. In "the admitted prior art," there is no suggestion that use by the execution stage (120) of the output from the instruction decoder (160) or the UOP cache (170) requires terminating the operation of the either the instruction cache (140), the instruction synchronization (150), or the instruction decoder (160).

Although their output may not be utilized by the execution stage (120) if the UOP cache (170) has a hit, the operations of the instruction cache (140), the instruction synchronization (150), and the instruction decoder (160) are otherwise unabated.

At least because "the admitted prior art" fails to disclose the "terminating" steps in claims 27 and 31, the claims are not anticipated. Withdrawal of the § 102(a) rejection is requested.

§ 102 Rejections - Claim 31

Claims 31 is rejected under 35 U.S.C. § 102(a) as being anticipated by Jourdan *et al.*, "eXtended Block Cache" ("Jourdan").

The Examiner asserts that terminating the operations of the instruction cache is "understood since an express purpose of utilizing the [trace cache] is to avoid if possible the latency involved with accessing un-decoded instructions via the instruction cache."

The Jourdan reference does not disclose of the "terminating" step in claim 31. As was demonstrated by the circuit illustrated in Figure 1 of Friendly, choosing to use data from the trace cache does not necessarily mean that the operations of the instruction cache are terminated. In this regard, Jourdan has the same deficiencies as the "admitted prior art" and Friendly. Withdrawal of the § 102(a) rejection is requested.

§ 103(a) Rejection - Claims 27 and 29

Claims 27 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Friendly in view of "the admitted prior art." Applicants respectfully submit that the combination of Friendly with "the admitted prior art" does not render obvious each limitation of the claims. For example, for reasons discussed above, neither Friendly nor "the admitted prior art" disclose the "terminating" steps recited in claims 27 and 29. Reconsideration and withdrawal of the § 103(a) rejection is requested.

§ 103(a) Rejection - Claims 34, 40, and 41

Claims 34, 40, and 41 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Friendly in view of U.S. Patent 5,913,223 to Sheppard *et al.* ("Sheppard").

For reasons discussed above, Friendly does not disclose the "terminating" step recited in independent claim 31, nor "the hit/miss indicator to selectively *disable* the data fetch unit" recited in independent claim 35. As the combination with Sheppard does not address the deficiencies of Friendly, Applicants submit that dependent claims 34, 40, and 41 are patentable at least as dependent limitations upon independent claims 31 and 35.

Conclusion

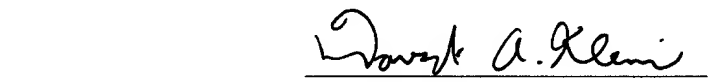
In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited.

Applicants authorize the Commissioner to charge any fees determined to be due with the exception of the issue fee and to credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,
KENYON & KENYON

Dated: April 14, 2005



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